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zeroing zeroed clear reset "selected data" mask

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Integrated content addressable memory array with processing ...

said response register contains all **zero** bits so that no CAM words are ... the **most significant bit** in said response register is cleared to read a next CAM ...

www.patentstorm.us/patents/5649149-claims.html - 34k - [Cached](#) - [Similar pages](#)

Associative memory system having configurable means for comparing ...

7 is a schematic diagram of a **zero** detect logic used in the detection of the to detect the next **most significant bit** satisfying the relationships, ...

www.patentstorm.us/patents/5444649-description.html - 60k - [Cached](#) - [Similar pages](#)

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Aligning load/store data using rotate, **mask**, **zero**/sign-extend and ...

The method may optionally include, performing **masking**, **zero**-extending and/or sign the lowest number and **most significant bit** being on the left, ...

www.freepatentsonline.com/7254699.html - 76k - [Cached](#) - [Similar pages](#)

Power up **clear** system for an electronic calculator or ...

6b there is shown the **mask** codes which are incorporated in many of the instruction ... Since a **zero** in the **most significant bit** (A.sub.10) in the program ...

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Configuration Parameters Dialog Box :: Running Simulations (Simulink)

Simulink defines **zero** crossings as consecutive if the time between events ... behavior at solver **reset** (e.g., after detecting a **zero** crossing) as follows: ...

www.mathworks.com/access/helpdesk/help/toolbox/simulink/ug/f11-35866.html - 142k -

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[PDF] Page 1 1 of 24 071107 FEATURES 16384 bits Electrically ...

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until a **reset** sequence is issued. All bits transferred to the DS2505 and received **zero** time slot it ensures that a read will occur before the fastest ...

www.maxim-ic.com/getds.cfm?qv_pk=2927 - [Similar pages](#)

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4 **Zero**-g level offset value after MSL3 preconditioning Data is transferred with the **Most Significant bit** (MSb) Solder **mask**. opening ...

www.st.com/stonline/products/literature/ds/12094.pdf - [Similar pages](#)

[PDF] COP313C Single-Chip CMOS Microcontrollers

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The **most significant bit** of Bd is not used to select a RAM. digit Hence each physical digit of RAM may Skip if G is **Zero**. 21. 0010 0001. (all 4 bits) ...

eshop.engineering.uiowa.edu/NI/pdfs/00/85/DS008537.pdf - [Similar pages](#)

[PDF] COP404C ROMless CMOS Microcontrollers

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ly of **mask**-programmed CMOS parts The COP404C is pri- can be enabled to output the **most significant bit** of SIO Skip if RAM Bit is **Zero** ...

www.sunmark.com/datasheets/cop404cn.pdf - [Similar pages](#)

[PDF] [Analog Output, High-Speed, 16-Bit, 12-Chan, PMC: Manual](#)

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CLEAR BUFFER clears automatically after the **reset** operation has been commences with the DAC in an all-zero state. The **most significant bit** initially ...

[www.generalstandards.com/download.php?](http://www.generalstandards.com/download.php?catid=usermanual&file=pmc16ao12_man_090406.pdf)

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